TUBF0320 Product Brief

1. Description

The TBUF0320 is a 20-output very-low-power clock buffer for PCIe 1.0/2.0/3.0/4.0/5.0/6.0, SAS, SATA, UPI and other applications.

It takes a reference input to fanout twenty 100MHz low-power differential HCSL outputs with on-chip terminations (integrated terminations for 85Ω transmission lines) that can save 80 external resistors and make layout easier. OE pins combined with SMBus bits, as well as a 3-wire side band interface, provide easier power management for each output. All OE pins are power down tolerant, which allows the OE pins to be driven by external signals when the device is in a power down or reset condition.

2. Features

- Supports Intel's DB2000QL spec
- 3.3V core and IO supply voltages
- Input Frequency: 100MHz (typ), up to 400MHz
- 20 differential low-power HCSL outputs with on-chip termination
- Two output enable control modes
- Traditional 8 OE# pins with power down tolerance and 20 SMBus bits
- Simple 3-wire Side-Band interface real-time control
- SMBus interface support
- 9 selectable SMBus addresses
- Spread spectrum tolerant
- Very low jitter outputs
- Differential additive phase jitter: DB2000Q<30fs RMS
- Differential additive phase jitter: PCIe 4.0<30fs RMS
- Differential additive phase jitter: PCIe 5.0<20fs RMS
- Differential additive phase jitter: PCIe 6.0<15fs RMS
- PCIe 1.0/2.0/3.0/4.0/5.0/6.0 compliant
- Cycle-to-cycle jitter < 50 ps
- Differential output-to-output skew < 50 ps
- Low propagation delay <3 ns
- Industrial temperature support: -40°C to 85°C
- 6 × 6 mm dual-row LGA80 package

3. Applications

- IT infrastructure (servers, storages)
- 5G communication
- Network system, including switches and routers
- Hardware accelerator

4. Functional Diagram

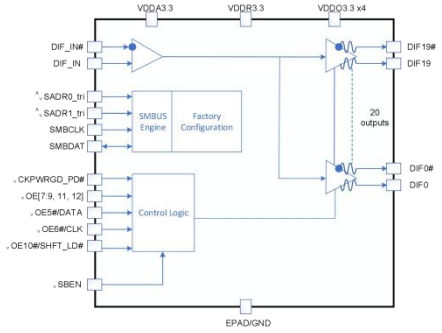

Figure 1 Functional Diagram